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Docket No.: 08211/0200254-US0
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Timothy Lance Blankenship

Patent No.: 6,970,033 B1

Issued: November 29, 2005

For: TWO-BY-TWO MULTIPLEXER CIRCUIT FOR COLUMN DRIVER

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.322

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted which should be corrected.

In the Specification:

Column 3, Line 24, Delete "(vgma 1-vgma 18)," and insert - - (vgma1-vgma18), - -.

Column 5, Line 51, Delete "(cnt1b)." and insert - - (cntlb). - -.

Column 5, Line 56, Delete "(in 1)" and insert - - (in1) - -.

Column 5, Line 63, Delete "(cnt1b)." and insert - - (cntlb). - -.

Column 6, Line 7, Delete "(cnt1b)," and insert - - (cntlb), - -.

Column 6, Line 19, Delete "po1b" and insert - - polb - -.

Column 6, Line 20, Delete "(cnt1b)." and insert - - (cntlb). - -.

Enclosed please find marked up copies of pages 4 and 8 of the specification.

The errors were not in the application as filed by applicant; accordingly no fee is required.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

Dated: January , 2006

Respectfully submitted,

By_____

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.	:	6,970,033 B1
APPLICATION NO.	:	10/723,280
ISSUE DATE	:	November 29, 2005
INVENTOR(S)	:	Timothy Lance Blankenship

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification:

Column 3, Line 24, Delete "(vgma 1-vgma 18)," and insert - - (vgma1-vgma18), - -.

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Column 6, Line 20, Delete "(cnt1b)." and insert - - (cntlb). - -.

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signal corresponds to a second logic level: each switch circuit is configured to turn on, and each tri-state inverter circuit is configured to provide a high-impedance output. The first switch circuit is configured to couple the first inverted signal to the second multiplexer output if the first switch circuit is on. Similarly, the second switch circuit is configured to couple the second inverted signal to the first multiplexer output if the second switch circuit is on.

FIG. 1 illustrates an example embodiment of a circuit (100) for an LCD. Circuit 100 includes a column driver circuit (102) and an LCD (104). One example column driver circuit 102 is a high-voltage column driver suitable for use in notebook LCD displays, desktop LCD monitors, LCD TV displays, and other applications.

Column driver circuit 102 is configured to drive LCD 104. As an example, column driver circuit 102 includes either a 6-bit or a 8-bit architecture, 384 - 480 outputs, and a 10V - 16V power supply (Vdda). Other embodiments of column driver circuit 102 may include other architectures.

In operation, column driver circuit 102 is configured to receive: (1) a polarity signal (pol), (2) a latch pulse signal (LP), (3) a data clock signal (CLKp/CLKn), (4) gamma reference voltages (vgma1-vgma18), and (5) data inputs (D00p/n - D23p/n). Column driver circuit 102 is responsive to signal pol to switch the polarity or voltage range of the column driver output. There are two polarity ranges, high range (e.g. from Vdda/2 to Vdda), and low range (e.g. from gnd to Vdda/2), wherein Vdda corresponds to a power supply voltage, and gnd is associated with a ground terminal.

FIG. 2 illustrates an example embodiment of a column driver circuit (200) that is arranged in accordance with aspects of the present invention. Column driver circuit 200 comprises a plurality of channels (e.g. sub-pixels) that are organized in pairs.

Each pair includes portion 210, a high-range decoder circuit (230), a low-range decoder circuit (232), a second multiplexer circuit (220), an input precharge circuit (240), two output amplifier circuits (250), and an output precharge circuit (260). Portion 210 includes a first multiplexer circuit (220).

High-range decoder circuit 230 is coupled between a first decoder node and a third multiplexer input node. Low-range decoder circuit 232 is coupled between a second decoder node and a fourth multiplexer input node. The second multiplexer circuit is

The first tri-state inverter circuit (402) is configured to receive a first multiplexer input signal (in1) at the first multiplexer input node (N1). The first tri-state inverter circuit (402) is also configured to receive a first control signal (cntl) and a complement of the first control signal (cntlb). The first tri-state inverter circuit (402) is also configured provide a first inverter output signal at the first switch node (N5) and a fifth switch node (N7) in response to the first multiplexer input signal, and provide the first inverter signal at the first inverter output node in response to the first multiplexer input signal (in1) if the first control signal (cntl) corresponds to a first logic level.

The second tri-state inverter circuit (404) is configured to receive a second multiplexer input signal (in2) at the second multiplexer input node (N2). The second tri-state inverter circuit (404) is also configured to receive the first control signal (cntl) and to receive the complement of the first control signal (cntlb). The second tri-state inverter circuit (404) is also configured to provide a second inverter output signal at the second switch node (N6) and a sixth switch node (N8) in response to the second multiplexer input signal (in2), and provide the second inverter signal at the second inverter output node in response to the second multiplexer input signal if the second control signal (cntl) corresponds to the first logic level.

The first switch circuit (412) is further coupled to the fifth switch node (N7). The first switch circuit (412) is configured to receive the first control signal (cntl) and the complement of the first control signal (cntlb), and provide the first inverter signal at the second multiplexer input node (N4) if the first control signal (cntl) corresponds to the second logic level. The second switch circuit (414) is further coupled to the sixth switch node (N8). The second switch circuit (414) is configured to receive the first control signal (cntl) and the complement of the first control signal (cntl), and to provide the second inverter signal at the first multiplexer output node (N3) if the first control signal (cntl) corresponds to the second logic level.

FIG. 5 illustrates an exemplary embodiment of the multiplexer circuit (220) of FIG. 4. Signal pol is used as the control signal (cntl), and signal polb is used as the complement of the control signal (cntlb). The first tri-state inverter circuit (402) is implemented with transistors M0-M3. The second tri-state inverter circuit (404) is implemented with transistors M19-M22. The first switch circuit (412) is implemented

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Telephone Number

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